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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,141	12/31/2003	Fernando Gonzalez	MICS:0114 (03-0027)	1749

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EXAMINER	
NGUYEN, JOSEPH H	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/751,141	GONZALEZ ET AL.	
	Examiner	Art Unit	
	Joseph Nguyen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election of claims 12-25 in the reply filed on 1/3/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the limitations "a depth in the range of approximately 300 A to 1500 A" in claims 13, 19, 23; "an aspect ratio of less than or equal to approximately 0.5 to 10" in claims 14, 20, 24; "an aspect ratio of less than or equal to approximately 1 to 3" in claims 15, 21, 52; "at a distance from the gate that is greater than 50% of the width of the respective drain and source terminals" in claim 16 are not supported by the disclosure.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 12 is rejected under 35 U.S.C. 102(e) as being anticipated by Michejda et al..

Regarding claim 12, Michejda et al. discloses on figure 1A a transistor comprising a drain terminal 178 comprising a doped polysilicon material (para [0049]) disposed within a first shallow cavity formed in an isolation oxide region; a source terminal 178 comprising a polysilicon material (para [0049]) disposed within a second shallow cavity formed in the isolation oxide region; a channel 130 formed in a silicon material and arranged between each of the first shallow cavity and the second shallow cavity, wherein the channel comprises a respective doped region (para [0041]) coupled to each of the drain terminal and the source terminal; and a gate 120 disposed over the channel and comprising one conductive layer disposed over a gate oxide layer 122.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 17, 18 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Michejda et al. in view of Tsuchiaki.

Regarding claim 17, Michejda et al. discloses on figure 1 substantially all the structure set forth in the claimed invention except a storage device. However, Tschuchiaki teaches about a storage device connected to a transistor (col. 1, lines 59-64). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Michejda et al. by having a storage device connected to a transistor for the purpose of utilizing the improved transistor in a memory cell.

Regarding claim 18, Tsuchiak teaches that the storage device comprises a capacitor (col. 1, lines 59-64).

Regarding claim 22, Michejda et al. discloses on figure 1 substantially all the structure set forth in the claimed invention except a memory device coupled to the processor and comprising a storage device. However, Tschuchiaki teaches about a memory device coupled to the processor (col.1, lines 42-45) and comprising a storage device (col. 1, lines 59-64). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Michejda et al. by having a memory device coupled to the processor and comprising a storage device for the purpose of utilizing the improved transistor in an integrated system in a single chip microcomputer.

Claims 13-15, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Michejda et al. as applied to claim 12 above.

Regarding claim 13, Michejda et al. discloses on figure 1 substantially all the structure set forth in the claimed invention except each of the plurality of cavities comprising a depth in the range of approximately 300A to 1500A. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Michejda et al. by having each of the plurality of cavities comprising a depth in the range of approximately 300A to 1500A for the purpose of improving the performance of a semiconductor transistor device, since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 14, Michejda et al. discloses on figure 1 substantially all the structure set forth in the claimed invention except each of the plurality of cavities comprising an aspect ratio of less than or equal to approximately 0.5 to 10. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Michejda et al. by having each of the plurality of cavities comprising an aspect ratio of less than or equal to approximately 0.5 to 10 for the purpose of improving the performance of a semiconductor transistor device, since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 15, Michejda et al. discloses on figure 1 substantially all the structure set forth in the claimed invention except each of the plurality of cavities comprising an aspect ratio of less than or equal to approximately 1 to 3. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Michejda et al. by having each of the plurality of cavities comprising an aspect ratio of less than or equal to approximately 1 to 3 for the purpose of improving the performance of a semiconductor transistor device, since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 16, Michejda et al. discloses on figure 1 substantially all the structure set forth in the claimed invention except each of the first and second conductive posts coupled to the respective drain and source terminals at a distance from the gate being greater than 50% of the width of the respective drain and source terminals. However, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify Michejda et al. by having each of the first and second conductive posts coupled to the respective drain and source terminals at a distance from the gate being greater than 50% of the width of the respective drain and source terminals for the purpose of improving the performance of a semiconductor transistor device, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claims 19-21, 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Michejda et al. and Tsuchiaki as applied to claims 17 and 22 above.

Regarding claims 19 and 23, Michejda et al. and Tsuchiaki discloses on figure 1 substantially all the structure set forth in the claimed invention except each of the plurality of cavities comprising a depth in the range of approximately 300A to 1500A. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Michejda et al. and Tsuchiaki by having each of the plurality of cavities comprising a depth in the range of approximately 300A to 1500A for the purpose of improving the performance of a semiconductor transistor device, since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims 20 and 24, Michejda et al. and Tsuchiaki substantially all the structure set forth in the claimed invention except each of the plurality of cavities comprising an aspect ratio of less than or equal to approximately 0.5 to 10. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Michejda et al. and Tsuchiaki by having each of the plurality of cavities comprising an aspect ratio of less than or equal to approximately 0.5 to 10 for the purpose of improving the performance of a semiconductor transistor device, since it has been held that where the general

conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims 21 and 25, Michejda et al. and Tsuchiaki disclose substantially all the structure set forth in the claimed invention except each of the plurality of cavities comprising an aspect ratio of less than or equal to approximately 1 to 3. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Michejda et al. and Tsuchiaki by having each of the plurality of cavities comprising an aspect ratio of less than or equal to approximately 1 to 3 for the purpose of improving the performance of a semiconductor transistor device, since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JN
February 2, 2005

ALLAN R. WILSON
PRIMARY EXAMINER